MOTOROLA
Semiconductor Products Inc.

AN-838
Application Note

HIGH PERFORMANCE MEMORY DESIGN TECHNIQUE FOR THE MC68000

This application note presents a technique for interfacing a 256K byte semi-transparent refresh memory board with an 8 MHz MC68000 microprocessor. The memory board consists of four banks of MCM6664 dynamic RAM chips and the memory control circuit. Each MCM6664 high-speed memory chip is provided with pin 1 refresh. To maintain RAM integrity, pin number 1 must be pulsed 128 times every 2 milliseconds. Moreover, each memory chip includes its own refresh counter/multiplexer and requires only 8 address (A0-A7) inputs. Thus, the MCM6664 chip is practically ideal for this task.

Semi-transparency, as used herein, means that the memory refresh cycle does not impact the system operational speed except for some special cases. System constraints determine whether these special cases do indeed occur. In effect, the system constraints determine the degree of refresh transparency. For a better understanding of the system constraint description, a brief look at the MCM6664 memory bank signal requirements is presented next.

MCM6664 MEMORY BANKS

Figure 1 identifies the signal requirements for the 4-bank memory portion of the semi-transparent refresh memory board. Buffering (not shown) is provided for all address, data, and control signals to the MC68000. During a write access (R/$\overline{W}$ low), the data byte active on the selected D0-D7 or D8-D15 inputs is stored at the memory location specified by the address inputs (A0-A7). During a read access (R/$\overline{W}$ high), a stored data byte from the address specified by the address lines is read out on the selected Q0-Q7 or Q8-Q15 data outputs.

Selection of the location to be accessed starts when a row address is active on the address lines and is latched into memory by the odd or even row address strobe ($\overline{RAS}$ EVEN or $\overline{RAS}$ ODD). Only the even $\overline{RAS}$ or the odd $\overline{RAS}$, never both, is active at any given time. This has the effect of activating only half of memory for an access at any given time. Then, the column address is made active on the address lines and is latched into memory by the applicable column address strobe ($\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$, or $\overline{CAS4}$). Note that $\overline{CAS1}$ and $\overline{CAS2}$ are assigned to the even word (even and odd byte) of memory, and $\overline{CAS3}$ and $\overline{CAS4}$ are assigned to the odd word (even and odd byte) of memory. This ensures that only half of memory is active during the entire access cycle. With the row and column addresses latched into memory, a data word is written into, or read out of, one of the 128K word locations in the selected memory bank.

The refresh odd ($\overline{REF\ ODD}$) signal can be applied to the odd banks while an even bank is being accessed and the opposite can occur with the refresh even ($\overline{REF\ EVEN}$) signal. In this manner, one location can be refreshed while the opposite location is being accessed. The even and odd memory banks must be refreshed 128 times every 2 milliseconds, respectively, for a total of 256 refresh pulses every 2 milliseconds.

SYSTEM CONSTRAINTS

In theory, the entire memory refresh should occur transparent to the system during the access of the opposite word, that is, a refresh of an even word during an odd word access and vice versa. In practice, the processor is not always accessing memory nor is the occurrence of an access predictable. Frequent accessing of memory can cause excess power dissipation by generating more refresh cycles than required for a given 2 millisecond period. These and other inherent memory refresh problems are resolved by the memory refresh control circuit.

MEMORY CONTROL CIRCUIT

Figure 2 is a schematic diagram of the control circuit portion of the memory board. This circuit decodes processor address and control signals and, in response, generates the required memory access control signals and the data transfer acknowledge ($\overline{DTACK}$) signal. Further, the circuit provides the memory refresh signals at the appropriate intervals to the appropriate half of memory.

Reference timing is provided by the 10 MHz crystal-

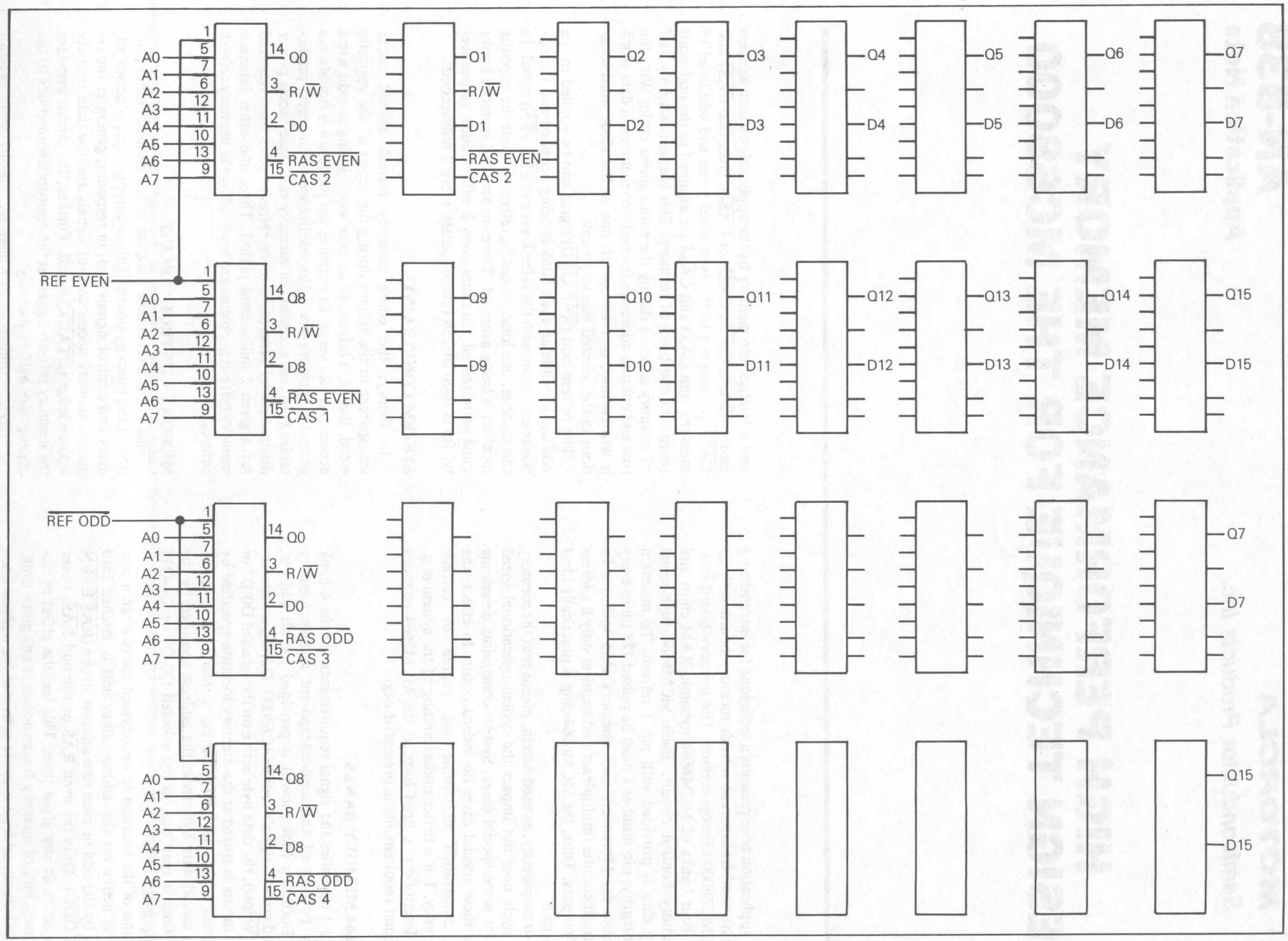

FIGURE 1 — MCM6664 Memory Bank Signals

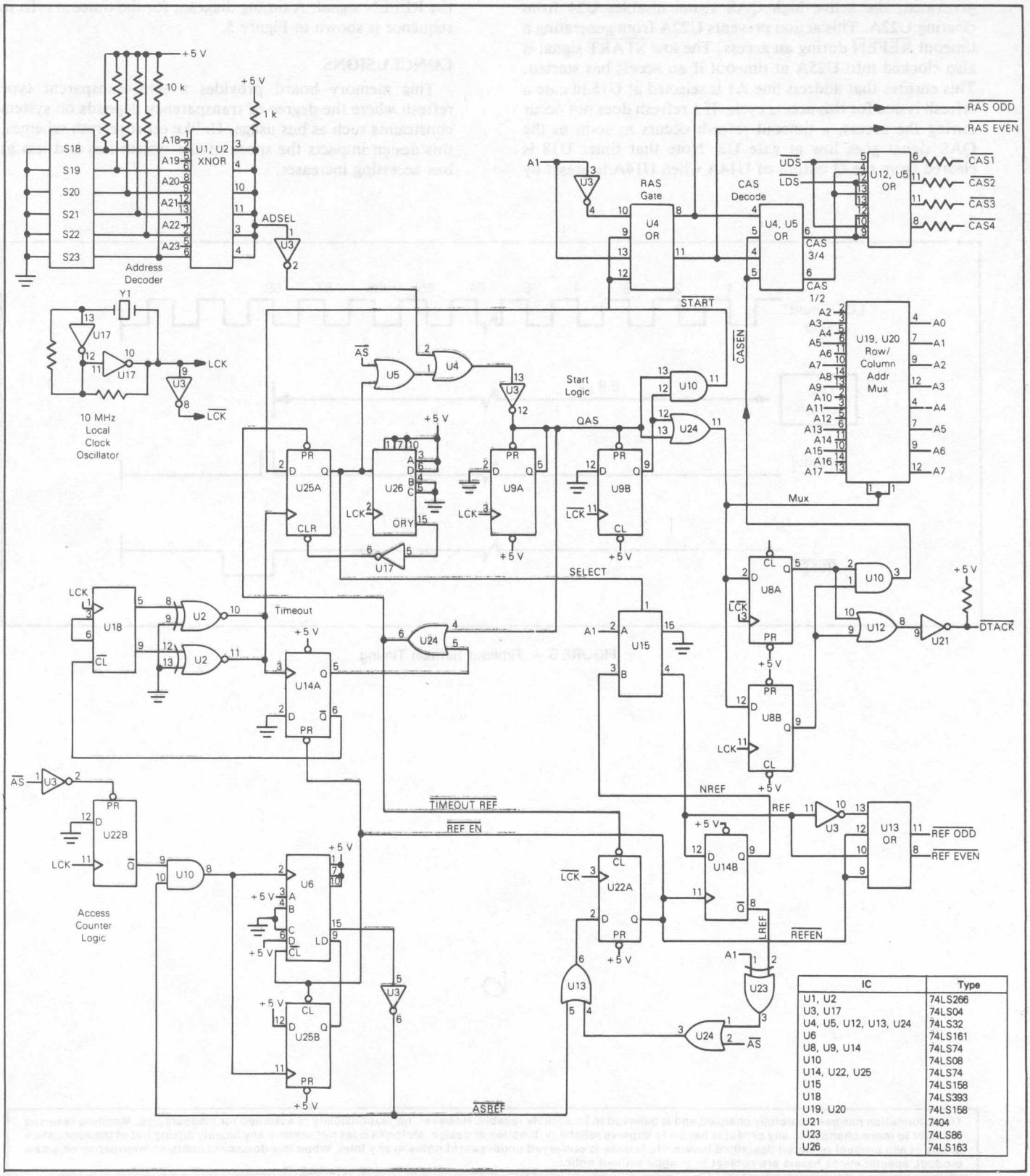

FIGURE 2 — Memory Access/Refresh Control Circuit Schematic Diagram

controlled local clock (LCK) oscillator Y1, U17. Two clock outputs, LCK and $\overline{LCK}$, allow clocking of the control circuit logic as close as 50 nanoseconds apart.

Address inputs include the address strobe ($\overline{AS}$), address lines A1-A23, and the upper and lower data strobes ($\overline{UDS}$, $\overline{LDS}$). The addressing scheme allows the memory board to be located anywhere in the MC68000 16 megabyte range as long as it is in a 256K boundary.

Address strobe ($\overline{AS}$) is sent by the processor to indicate that the address lines are valid. This signal is used by the control circuit to start an access cycle and to keep track of accesses.

Address line A1 is used to generate the odd (A1 high) or even (A1 low) row address strobes ($\overline{RAS}$ ODD or $\overline{RAS}$ EVEN). If refresh occurs during an access, A1 also determines the polarity of the refresh signal. Signals $\overline{UDS}$ and $\overline{LDS}$ are used in conjunction with address line A1 to select one of the four column address strobes ($\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$, or $\overline{CAS4}$).

Address lines A2-A9, when active, contain the row address, and lines A10-A17, when active, contain the column adress. The row and column address lines are multiplexed at U19, U20 to provide the memory address (A0-A7). The MUX signal input to U19, U20 from U24 is used to select the A2-A9 (MUX high) inputs or the A10-A17 (MUX low) inputs.

Address lines A18-A23 are used to decode the memory board address. When active, this address alerts the control circuit that the processor wants to access this particular memory board. Switches S18-S22 are preset to the address assigned to the memory board and are compared with address lines A18-A23 at exclusive NOR gates U1, U2. When a match occurs at these gates, the address select (ADSEL) signal goes high and is applied to gate U4 as a low via inverter U3. At this time, address lines A1-A17 are also active. The MUX input to U19, U20 is high, placing the A2-A9 row address on the A0-A7 output lines. Line A1 is active at the input of $\overline{RAS}$ gates U4. However, U4 is disabled by the high $\overline{START}$ input from AND gate U10 because flip-flop U9 is in the preset state. The only thing needed now to start an access cycle is the $\overline{AS}$ signal.

ACCESS CYCLE OPERATION

Signal $\overline{AS}$ is issued by the processor after the address bus has become valid, allowing some buffering and address decoding time to expire. When $\overline{AS}$ goes low, gate U4 is enabled and ADSEL is applied to the preset inputs of U9 as the high qualified address strobe (QAS). This signal releases U9 and the next rising edge of either LCK or $\overline{LCK}$ toggles half of U9 to a low output state. This action generates the U10 low $\overline{START}$ output to enable the $\overline{RAS}$ gates and allows the row address to be latched into memory. In effect, the odd or even $\overline{RAS}$ is generated on the first clock edge following $\overline{AS}$ as shown on the timing diagram in Figure 3. Fifty nanoseconds later, the next clock edge toggles the other half of U9 and switches the U24 MUX signal from high to low to place the column address at the output of U19, U20. The low MUX signal is also applied to the D inputs of U8, so the next clock edge, after MUX goes low, toggles half of U8. This action enables the $\overline{CAS}$ gates, and with the $\overline{UDS}$ or $\overline{LDS}$ signal active, $\overline{CAS}$ is generated to latch the column address into memory. The next edge of the clock toggles the other half of

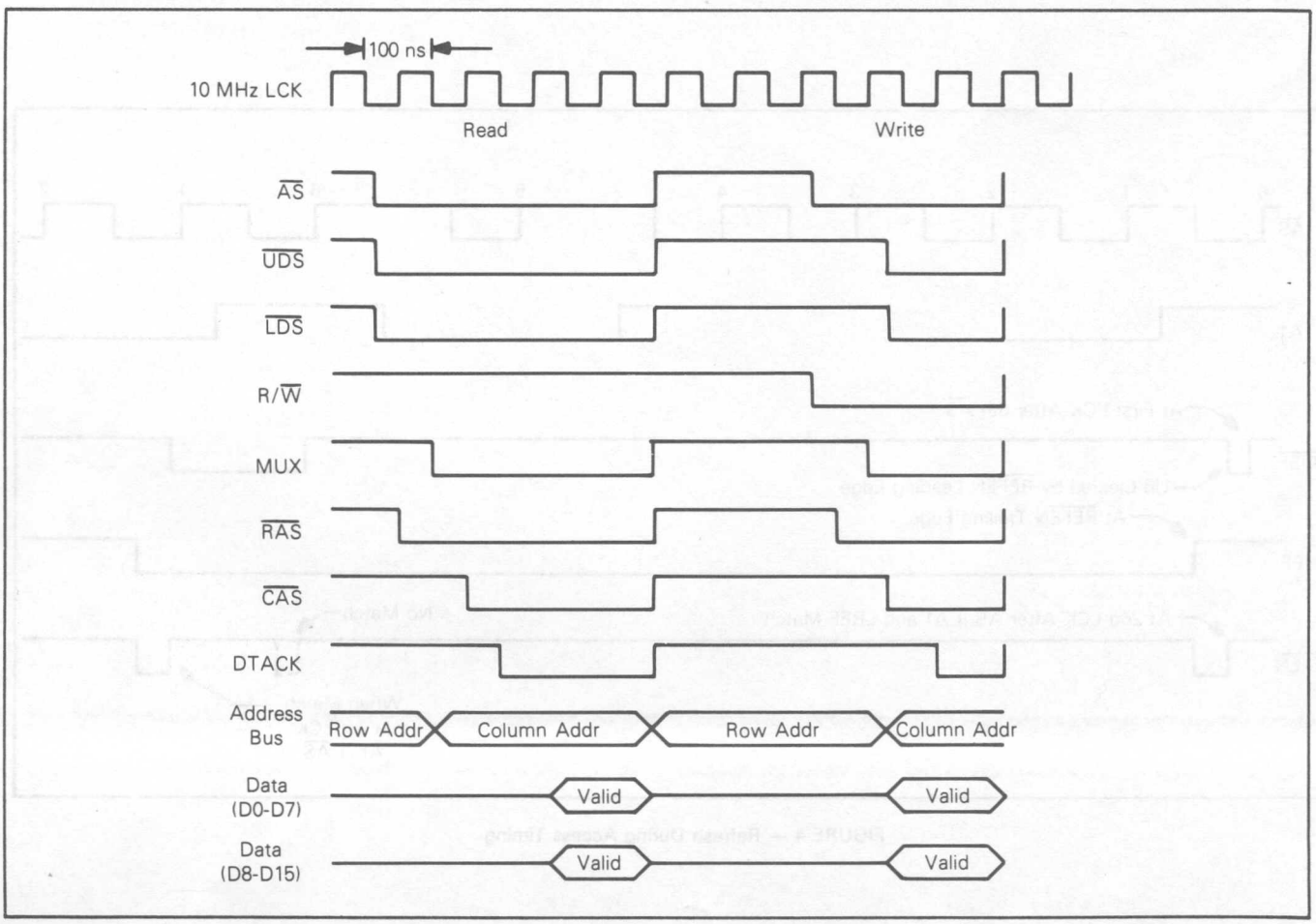

FIGURE 3 — Access Cycle Timing Diagram

U8 and generates $\overline{\text{DTACK}}$. Note on Figure 3 that $\overline{\text{RAS}}$, MUX, $\overline{\text{CAS}}$, and $\overline{\text{DTACK}}$ occur in a 50 nanosecond sequence. This timing ensures that each event has its allotted hold time and occurs in the proper sequence. For example, this timing meets the $\overline{\text{DTACK}}$-to-DATA specification number 47 requirements. This specification requires $\overline{\text{DTACK}}$ to precede data by no more than 90 nanoseconds. Signal $\overline{\text{CAS}}$ is used for access only and is negated by $\overline{\text{RAS}}$. Refresh can occur during frequent or infrequent accessing as described in the following paragraphs.

REFRESH DURING AN ACCESS

During frequent accessing (more than 6 accesses within 6.8 microseconds), a refresh cycle is initiated by counter U6 after detecting 6 successive $\overline{\text{AS}}$ signals. The input logic to U6 detects $\overline{\text{AS}}$ on the rising edge of LCK at U22B to synchronize the refresh cycle with the access cycle. After detecting the sixth AS, U6 generates the address strobe refresh ($\overline{\text{ASREF}}$) signal. Signal $\overline{\text{ASREF}}$ is routed via U13 to the D input of U22A. The next rising edge of LCK toggles U22A to generate the low refresh enable ($\overline{\text{REFEN}}$) signal. At this time, the refresh (REF) signal out of inversion multiplexer U15, is present at the odd or even refresh output gates. The REF signal, during an access cycle, is the inverted address line A1 since the A1 input to U15 is selected by the output of flip-flop U25A. In this manner, the $\overline{\text{REFEN}}$ signal strobes out the $\overline{\text{REF ODD}}$ or $\overline{\text{REF EVEN}}$ signals at the same time that the $\overline{\text{RAS}}$ signal is active on the opposite word of the memory. The $\overline{\text{REFEN}}$ signal performs other functions. It clears the $\overline{\text{AS}}$ counter logic and the timeout logic (described later) and clocks refresh status register U14B. When the $\overline{\text{AS}}$ counter is cleared by $\overline{\text{REFEN}}$, the next LCK sends $\overline{\text{REFEN}}$ high, more than meeting the low 60 nanosecond refresh signal requirement. The input to U14B is the REF output from U15. Therefore, when clocked by REFEN, U14B stores the polarity of the refresh signal. The U14B next refresh (NREF) output is selected as the U15 input during a timeout refresh. A last refresh (LREF) output from U14B is exclusive ORed with address line A1 during an access cycle to ensure that the next refresh is of the correct polarity. If not of the correct polarity, the $\overline{\text{ASREF}}$ input to U22A is inhibited at gate U3 until a match is obtained between address line A1 and LREF. A timing diagram depicting the $\overline{\text{AS}}$, A1, $\overline{\text{ASREF}}$, LREF, and REFEN signal relationship is shown in Figure 4.

REFRESH DURING TIMEOUT

During infrequent accessing (less than 6 accesses within 6.8 microseconds), watchdog timer U18 counts 68 LCK pulses and generates the TIMEOUT signal at U2. This signal clocks U25A and U14A. A low U14A output enables gate U24 and if QAS is low (no access started), U24 presets U25A to a high output. This high selects the NREF input to U15 as the REF signal. U24 also clears U22A to generate the REFEN signal. This action generates the required REF ODD or REF EVEN signal. Note that the output of U25A is tied to timer U26 and to AS gate U5. When the U25A output goes high at timeout refresh, a high is applied to AS gate U5 to inhibit AS from being recognized. The high U25A output also starts timer U26. After 600 nanoseconds, timer U26 clears U25A to enable AS gate U5. This action ensures the memory specification requirement that an access cannot occur for 460 nanoseconds after MCM6664 refresh pin number 1 has been pulled low.

If an access has already started when the timeout signal is

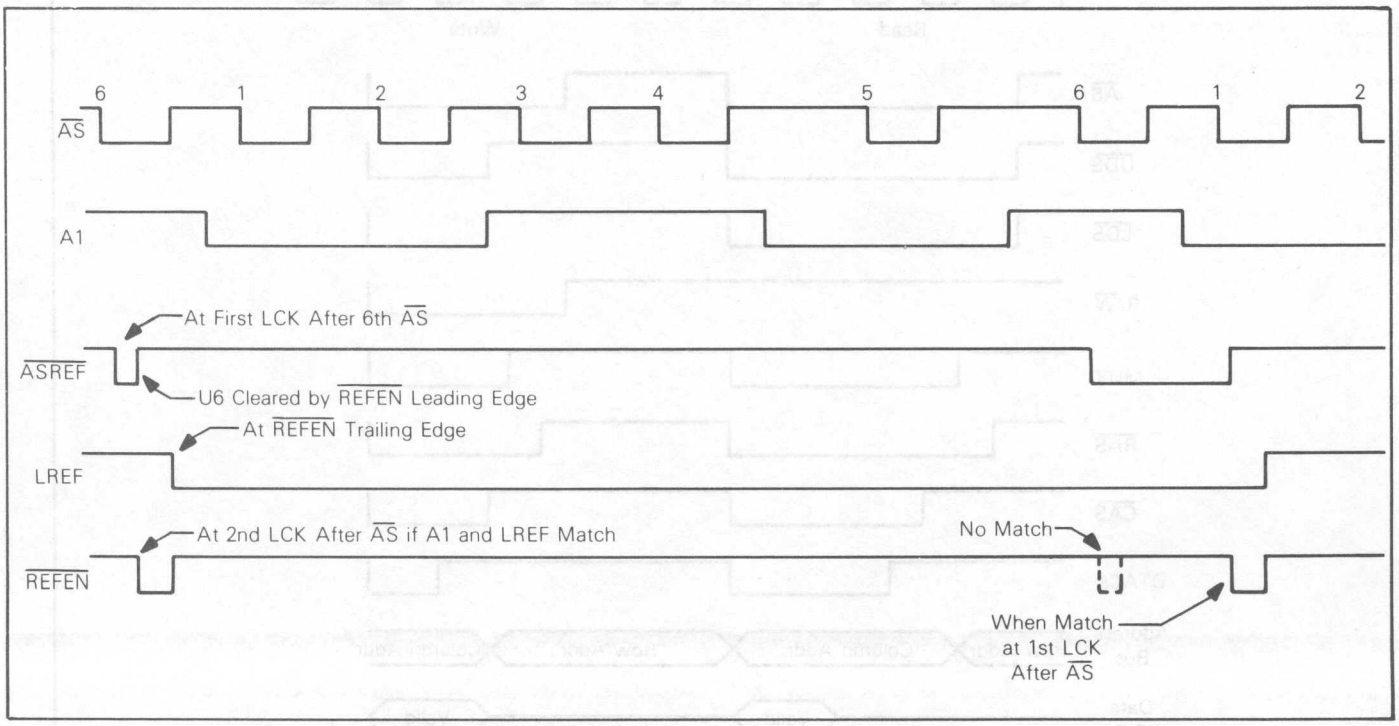

FIGURE 4 — Refresh During Access Timing

generated, the active high QAS signal disables U24 from clearing U22A. This action prevents U22A from generating a timeout $\overline{\text{REFEN}}$ during an access. The low $\overline{\text{START}}$ signal is also clocked into U25A at timeout if an access has started. This ensures that address line A1 is selected at U15 in case a refresh is due for this access cycle. If a refresh does not occur during the access, a timeout refresh occurs as soon as the QAS signal goes low at gate U2. Note that timer U18 is cleared from the $\overline{Q}$ output of U14A when U14A is preset by the $\overline{\text{REFEN}}$ signal. A timing diagram for the timeout refresh sequence is shown in Figure 5.

CONCLUSIONS

This memory board provides a semi-transparent type refresh where the degree of transparency depends on system constraints such as bus usage. Unlike other refresh schemes, this design impacts the speed of the system less and less as bus accessing increases.

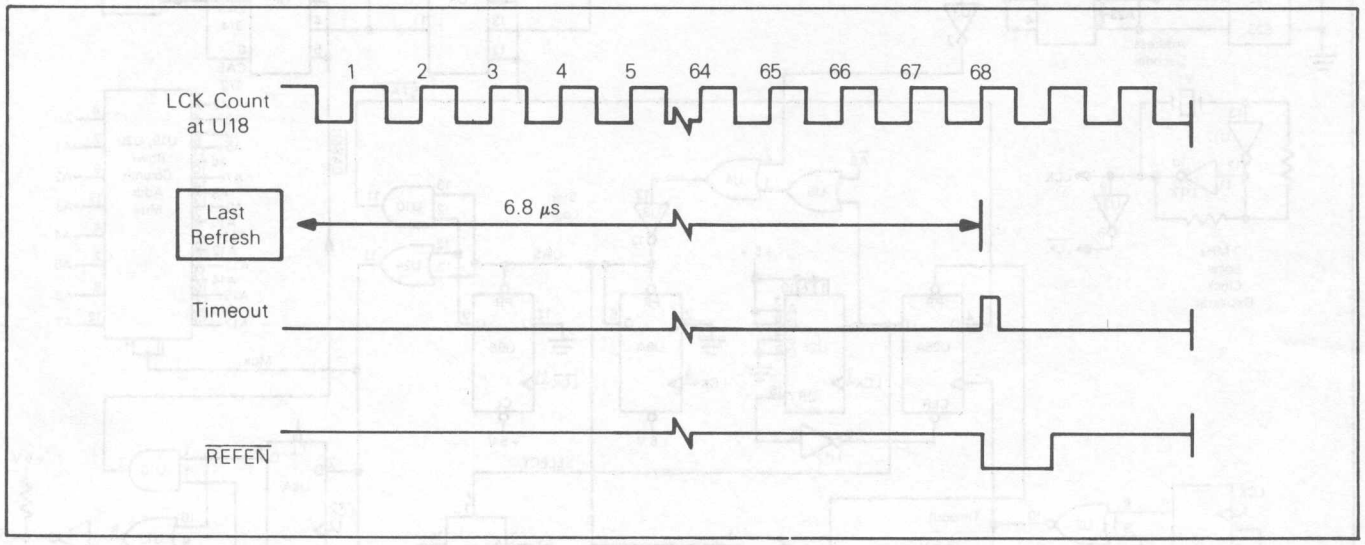

FIGURE 5 — Timeout Refresh Timing

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